CLAIMS

1. (Original) A method of forming a diode for integration with a semiconductor device comprising the steps of:

providing a layer of semiconductor material;

forming a dielectric layer over the layer of semiconductor material;

introducing a first conductivity type dopant into the dielectric layer;

forming a semi-conductive layer over the dielectric layer;

introducing a second conductivity type dopant into a first region of the semi-conductive layer; and

re-distributing the first conductivity type dopant from the dielectric layer into the semi-conductive layer so as to form a second region of the first conductivity type dopant in the semi-conductive layer, the second region being adjacent the first region so as to provide a P/N junction of the diode.

2. (Currently amended) ~~The method according to claim 1~~ A method of forming a diode for integration with a semiconductor device comprising the steps of:

providing a layer of semiconductor material;

forming a dielectric layer over the layer of semiconductor material;

introducing a first conductivity type dopant into the dielectric layer;

forming a semi-conductive layer over the dielectric layer;

introducing a second conductivity type dopant into a first region of the semi-conductive layer; and

re-distributing the first conductivity type dopant from the dielectric layer into the semi-conductive layer so as to form a second region of the first conductivity type dopant in the semi-conductive layer, the second region being adjacent the first region so as to provide a P/N junction of the diode,

wherein the re-distributing step comprises heating the semiconductor device to diffuse the first conductivity type dopant into the semi-conductive layer.

3. (Original) The method according to claim 1 wherein the step of providing a layer of semiconductor material comprises the step of providing an epitaxial layer.

4. (Cancelled).

5. (Currently amended) ~~The method according to claim 4~~ A method of forming a diode for integration with a semiconductor device comprising the steps of:

providing a layer of semiconductor material;

forming a dielectric layer over the layer of semiconductor material;

introducing a first conductivity type dopant into the dielectric layer;

forming a semi-conductive layer over the dielectric layer;

introducing a second conductivity type dopant into a first region of the semi-conductive layer;

forming a cap layer over the semi-conductive layer;

re-distributing the first conductivity type dopant from the dielectric layer into the semi-conductive layer so as to form a second region of the first conductivity type dopant in the semi-conductive layer, the second region being adjacent the first region so as to provide a P/N junction of the diode,

wherein the step of forming a cap layer occurs before the re-distributing step;

forming first and second openings in the cap layer extending to the first and second regions of the semi-conductive layer; and

forming contacts in the first and second openings to the first and second regions of the semi-conductive layer.

6. (Currently amended) The method according to claim ~~4~~5 wherein the cap layer comprises at least one dielectric layer.

7. (Original) The method according to claim 1 wherein the step of forming a semi-conductive layer comprises the step of forming a layer of one of the following materials: polysilicon, and oxygen doped polycrystalline silicon (SIPOS).

8. (Original) The method according to claim 1 wherein the step of introducing a second conductivity type dopant comprises the steps of:

forming a mask over the semi-conductive layer;

removing a portion of the mask so as to expose the first region of the semi-conductive layer; and

implanting the second conductivity type dopant into the first region of the semi-conductive layer.

9. (Original) A method of forming a transistor device having an integrated diode, the method comprising the steps of:

providing a layer of semiconductor material;

forming a first dielectric layer over the layer of semiconductor material having a first thickness;

introducing a first conductivity type dopant into the first dielectric layer;

patterning the first dielectric layer so as to provide an opening in the first dielectric layer extending to the layer of semiconductor material, the opening forming an active area of the transistor device;

forming a second dielectric layer over the layer of semiconductor material in the active area having a second thickness, the first thickness being greater than the second thickness;

forming a semi-conductive layer over the first and second dielectric layers;

introducing a second conductivity type dopant into the semi-conductive layer over the active area and into a first region of the semi-conductive layer over the first dielectric layer;

forming a cap layer over the non-conductive region;

forming openings extending through the cap layer, and semi-conductive layer to the second dielectric layer in the active area and to the first dielectric layer;

introducing a dopant of the first conductivity type into the layer of semiconductor material through the openings in the active area;

re-distributing the first conductivity type dopant from the first dielectric layer into the semi-conductive layer over the first dielectric layer so as to form a second region of the first conductivity type dopant in the semi-conductive layer, the second region being adjacent the first

region so as to provide a P/N junction of the integrated diode and re-distributing the dopant of the first conductivity type in the layer of semiconductor material so as to form regions of the first conductivity type in the semiconductor material;

introducing a dopant of the second conductivity type into the regions of the first conductivity type to form a source region of the transistor device; and

forming contacts to the source region, and the first and second regions.